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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,881	09/23/2003	Robin E. Gorrell	58053US005	3599

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EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

NOTIFICATION DATE	DELIVERY MODE
10/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/668,881	GORRELL ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on August 1, 2007 has been received and entered in the case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. (U. S. Pat. No. 5,354,955) in view of Hanson et al. (U. S. Pat. No. 4,496,793).

Regarding claim 1, Gregor et al. discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

- a substrate (12; column 3, line 7) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that define contact pads (the pads under the solder ball 20 and pads on the top surface of the substrate 12) for attachment to corresponding pads on the chip (14; column 3, line 8) and board (10; column 3, line 5),
- wherein the board attach surface (at the bottom surface of the substrate 12) comprises

- a pattern of contact pads (the pads under the solder ball 20) opposite and "adjacent" a chip attach location (the area on the substrate 12 where the chip 14 is attached) on the chip attach surface except at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of the board attach surface (see e.g., Fig. 1),
- said unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being "adjacent" to a corner of chip attach location (see e.g., Fig. 1), and

- said board attach surface (the surface that has the elements 120) comprising a dielectric material (the lowermost dielectric layer in the element 12). As shown in e.g., Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region. Gregor et al. doesn't explicitly state that the unpatterned solid plane area is at least the size at which the strain is less then the cracking strain in the thermal cycling from 125°C to -55°C. The stresses are related to the types of materials and other parameters i.e., the die size and thickness, substrate thickness, etc. (see page 12, lines 27 – 30 of the specification of instant invention), so in a device where a crack does not occur, it can be assumed that the size is greater than the size at which the strain causes a crack, as if it weren't then the crack would occur.

Mils SPEC Std 202 specifies that devices should operate without failures in solder joints from -55°C to +125°C. Therefore, one of ordinary skill would have found reason, motivation and suggestion to select the material so that no cracking occurs in cycling over the operating range of -55°C to +125°C. In designing a device to exceed the standard for Mil standard 202, the lack of cracking would inherently require the absence of cracking, which would mean for the size of the unpatterned area was large enough that no cracking accurs. Furthermore, it is a common knowledge that reducing thermal stress or thermal mismatch prevents cracking in the substrate (see column 7, line 66 – column 8, line 6 of Arai et al.).

To withstand common standard thermal stress cycles, the multi-layer board must withstand more than 400 thermal stress cycles to meet Mil Std 202. Inherently, any multi-layer board withstood the more than 400 thermal stress cycles per Mil Std 202 which is thermal cycling of assembled circuits between -55°C to +125°C with no failures in solder joins. Thus, the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of Gregor et al. would withstand the common standard thermal stress cycles.

Alternatively, not relying of Gregor et al.'s disclosure that the limitation "the unpatterned solid plane area being at least the size of a region in which strain due to thermal cycling from 125°C to – 55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area" is taught by Hanson et al. in e.g., column 4, lines 54 – 65 an entire area of a circuit board withstanding more than strain due to thermal cycling from 125°C to –

55°C without cracking or failures. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the circuit board that withstands more than strain due to thermal cycling from 125°C to – 55°C without cracking or failures of Hanson et al. to be the substrate of Gregor et al. as taught by Hanson et al. to produce an average thermal coefficient of expansion of approximately $8.9 * 10^{-6}$ inch per inch per degree Celsius (column 4, lines 57 – 60).

Regarding claim 4, Gregor et al. discloses in e.g., Fig. 1 a laminated flip-chip interconnect package (the package in Fig. 1) comprising

- a substrate (12) having a chip attach surface (the top surface of the substrate 12 where the chip 14 is attached) and an opposing board attach surface (the bottom surface of the substrate 12) that defines a pattern of contact pads (the pads between the solder ball 20 and the substrate 12) for attachment to corresponding pads on the chip (14) and board (10),
- wherein the board attach surface (at the bottom surface of the substrate 12) comprises
    - at least one unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25),
    - said unpatterned area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) being opposite a chip attach surface region adjacent at least one corner of a chip attach location (see e.g., Fig. 1), and

- said board attach surface comprising a metal (At the year 1994, all wirings or circuits or pads materials includes metal materials, i.e., copper or aluminum, etc. Thus, Gregor et al. meets this limitation.). As shown in e.g., Fig. 1 of Gregor et al., the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) has at least the size of a region. Furthermore, to withstand common standard thermal stress cycles, the multi-layer board must withstand more than 400 thermal stress cycles per Mil Std 202. Inherently, any multi-layer board withstood the more than 400 thermal stress cycles per Mil Std 202 which is thermal cycling of assembled circuits between –55 and 125 degrees Celsius with no failures in solder joins. Thus, the unpatterned solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) of Gregor et al. would withstand the common standard thermal stress cycles.

Alternatively, not relying of Gregor et al.'s disclosure that the limitation "the unpatterned solid plane area being at least the size of a region in which strain due to thermal cycling from 125°C to – 55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area" is taught by Hanson et al. in e.g., column 4, lines 54 – 65 an entire area of a circuit board withstanding more than strain due to thermal cycling from 125°C to – 55°C without cracking or failures. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the area of the circuit board that withstands more than strain due to thermal cycling from 125°C to – 55°C without cracking or failures of Hanson et al. into the substrate of Gregor et al. as taught by Hanson et al. to produce an average

thermal coefficient of expansion of approximately 8.9 * 10^{-6} inch per inch per degree Celsius (column 4, lines 57 – 60).

4. Claims 2, 3 and 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregor et al. and Hanson et al. as applied to claims 1 and 4 above, and further in view of Lau (U. S. Pat. No. 6,075,710).

Regarding claims 2, 3 and 5 – 7, while Gregor et al. and Hanson et al. disclose the use of the dielectric and metal materials on the board attach surface of the substrate, Gregor et al. and Hanson et al. do not disclose a solder mask on the dielectric material (claim 2) and metal (claim 6), the solder mask being a polyimide (claims 3 and 7) and the metal material being copper (claim 5). Lau teaches in e.g., Fig. 4A a solder mask (155 or 235; column 5, lines 65 – 67) on a dielectric material (the dielectric material in the bottom of the substrate; column 5, lines 19 and 20) and metal (Cu 130; column 5, lines 38 – 40) and the solder mask being a polyimide (column 7, line 39. Since the element 235 of Lau works as a mask layer for the solder pastes 245, the element 235 reads as a solder mask. Since the solder mask 235 is made by a polyimide material, Lau discloses a polyimide material for the solder mask). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to further apply the solder mask (e.g., polyimide) of Lau to cover the dielectric material and metal on the unpatterned solid plane area of Gregor et al. and Hanson et al. as taught by Lau to provide finer pitches between the external connections (column 6, lines 4 – 6).

Regarding claim 8, Gregor et al., as modified, discloses a solder mask (155 of Lau) having a plurality of openings (the openings for the pads 130 of Lau) defining ball grid array pads (see e.g., Fig. 3C).

Response to Arguments

5. Applicant's arguments filed on August 1, 2007 have been fully considered but they are not persuasive.

On page 7, applicant argues "Applicants requests the Examiner to provide the basis on which the assumption is made that the absence of a crack in Gregor is achieved by the present invention rather than other solutions such as the internal metalized stabilizing layers of Hanson, which is cited by the Office Action." Since applicant merely argues against Gregor in a general manner rather than pointing out specific structural differences, the argument is not persuasive.

Furthermore, applicant argues "nothing in Gregor indicates that it is trying to exceed Mil standard 202, which is military specification, so it would not be known if the device in Gregor would exceed Mil standard 202." This argument is not persuasive because applicant does not provide any factual evidence that is required to rebut a prima facie case of obviousness. In other words, attorney's argument is not evidence unless it is an admission.

Even further, applicant argues "the cited references do not provide a motivation or suggestion for an unpatterned solid plane area on the board attach surface." This argument is not persuasive. Contrary to applicant's assertion and as stated in the rejection, motivation was established by Hanson et al., specifically in column 4, lines 57 – 60 (to produce an average thermal coefficient of expansion of approximately $8.9 * 10^{-6}$ inch per inch per degree Celsius).

Applicant should note that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Next, applicant argues "the stabilizing layers of Hanson are not a solid plane, but instead have enlarged apertures filled with epoxy resin ... Therefore, the combination of the teachings of Hanson and Gregor still would not disclose or provide motivation for the present invention." Such argument is not persuasive because Hanson discloses in e.g., Fig. 3 and column 4, lines 44 – 50 a complete laminate structure having the electrical connections by drilling and plating of thru holes. Also, inherently, any epoxy resin is cured at room temperature. Thus, the final product of the stabilizing layers of Hanson is a solid plane. Therefore, the combination of the teachings of Hanson and Gregor is proper and would disclose or provide motivation for the present invention.

Finally, applicant argues "these references ... do not disclose an unpatterned solid plane area on the board attach surface adjacent to a corner of a chip attach location, wherein the unpatterned solid plane area is at least size of a region in which strain due to thermal cycling from 125°C to – 55°C is greater than the strain at which cracking will occur in the absence of the unpatterned solid plane area." As explained in the above, since applicant merely argues against Gregor and Hanson in a general manner rather than pointing out specific structural differences, the argument is not persuasive. Furthermore, since Gregor and Hanson provides the unpatterned

solid plane area (at the solid and non-pad areas on the back surface of the element 12 which are directly opposite areas of the element 25) on the board and the chip (14) in the physical arrangement as claimed, it is considered to meet the structural limitations of the claim and the arguments clearly fail to distinguish the claimed invention from the disclosure of Gregor and Hanson.

For the above reasons, the rejection is maintained.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

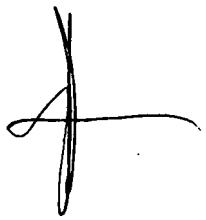
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chris C. Chu
Examiner
Art Unit 2815



c.c.
Thursday, September 20, 2007

KENNETH PARKER
SUPERVISORY PATENT EXAMINER